PATENT
Attorney Docket No. ASC-058B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Leitz *et al.*		
SERIAL NO.:	10/646,353	GROUP NO.:	2811
FILING DATE:	August 22, 2003	EXAMINER:	Not Yet Assigned
TITLE:	Semiconductor Heterostructures Having Reduced Dislocation Pile-Ups and Related Methods		

CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23rd day of December, 2003.

Emily Walsh

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

1. Transmittal Form (1 pg.);
2. Information Disclosure Statement (2 pgs.);
3. Form PTO-1449 (17 pgs.), with copies of cited references B1-B48 and C1-C131;
4. Return Receipt Postcard; and this
5. Certificate of First Class Mailing (1 pg.).

2725505

TRANSMITTAL FORM

Application Serial Number	10/646,353
Filing Date	August 22, 2003
First Named Inventor	Leitz
Group Art Unit	2811
Examiner Name	Not Yet Assigned
Attorney Docket No.	ASC-058B
Patent No.	Not Applicable
Issue Date	Not Applicable

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Check Attached
  - ☐ Copy of Fee Transmittal Form
- ☐ Amendment/Response
  - ☐ Preliminary
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
  - ☐ Letter to Official Draftsperson including Drawings [Total Sheets _____]
- ☐ Petition for Extension of Time
- ☒ Information Disclosure Statement
  - ☒ Form PTO-1449
  - ☒ Copies of IDS Citations (B1-B48 and C1-C131)
- ☐ Certified Copy of Priority Document(s)
- ☐ Sequence Listing submission
  - ☐ Paper Copy/CD
  - ☐ Computer Readable Copy
  - ☐ Statement verifying identity of above
- ☐ Copy of Notice to File Missing Parts of Application
- ☐ Formal Drawing(s)
- ☐ Request For Continued Examination (RCE) Transmittal
- ☐ Power of Attorney (Revocation of Prior Powers)
- ☐ Terminal Disclaimer
- ☐ Executed Declaration and Power of Attorney for Utility or Design Patent Application
- ☐ Small Entity Statement
- ☐ CD(s) for large table or computer program
- ☐ Amendment After Allowance
- ☐ Request for Certificate of Correction
  - ☐ Certificate of Correction (in duplicate)
- ☐ Notice of Appeal to Board of Patent Appeals and Interferences
- ☐ Appeal Brief (in triplicate)
- ☐ Status Inquiry
- ☒ Return Receipt Postcard
- ☒ Certificate of First Class Mailing under 37 C.F.R. 1.8
- ☐ Certificate of Facsimile Transmission under 37 C.F.R. 1.8
- ☐ Additional Enclosure(s) *(please identify below)*

CORRESPONDENCE ADDRESS

Direct all correspondence to:

Patent Administrator
Testa, Hurwitz & Thibeault, LLP
High Street Tower
125 High Street
Boston, MA 02110
Tel. No.: (617) 248-7000
Fax No.: (617) 248-7100

SIGNATURE BLOCK

Respectfully submitted,

Date: December 23, 2003
Reg. No. 50,773
Tel. No.: (617) 248-7453
Fax No.: (617) 248-7100

Mark L. Belgorodov
Attorney for Applicants
Testa, Hurwitz & Thibeault, LLP
High Street Tower
125 High Street
Boston, MA 02110

2725508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Leitz *et al.*

SERIAL NUMBER: 10/646,353 ART UNIT: 2811

FILING DATE: August 22, 2003 EXAMINER: Not Yet Assigned

TITLE: Semiconductor Heterostructures Having Reduced Dislocation Pile-Ups and Related Methods

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98 (a)(2)(i), only copies of the foreign patent documents and non-patent publications are enclosed.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

In addition, Applicants wish to inform the Examiner about the following commonly-owned, co-pending patent applications, including all cited references and Office actions issued therein:

U.S. Serial Number	Filing Date	Inventor Name
09/611,024	July 6, 2000	Fitzgerald
10/268,025	October 9, 2002	Fitzgerald
10/268,425	October 10, 2002	Vineis et al.

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed before the mailing of the first Office action on the merits. Applicants believe no fees are due for this paper to be entered and considered, but the Commissioner is hereby authorized to charge Deposit Account No. 20-0531 for any required fees that may be due.

Respectfully submitted,

Date: December 23, 2003
Reg. No. 50,773

Mark L. Beloborodov
Attorney for Applicants
Testa, Hurwitz & Thibeault, LLP
High Street Tower
125 High Street
Boston, MA 02110

Tel. No.: (617) 248-7453
Fax No.: (617) 248-7100

2725546

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	2001/0003364	06/14/2001	Sugawara *et al.*			
	A2	2001/0014570	08/16/2001	Wenski *et al.*			
	A3	2002/0043660	04/18/2002	Yamazaki *et al.*			
	A4	2002/0052084	05/02/2002	Fitzgerald			
	A5	2002/0084000	07/04/2002	Fitzgerald			
	A6	2002/0096717	07/25/2002	Chu *et al.*			
	A7	2002/0100942	08/01/2002	Fitzgerald *et al.*			
	A8	2002/0123167	09/05/2002	Fitzgerald			
	A9	2002/0123183	09/05/2002	Fitzgerald			
	A10	2002/0123197	09/05/2002	Fitzgerald *et al.*			
	A11	2002/0125471	09/12/2002	Fitzgerald *et al.*			
	A12	2002/0125497	09/12/2002	Fitzgerald			
	A13	2002/0168864	11/14/2002	Cheng *et al.*			
	A14	2002/0185686	12/12/2002	Christiansen *et al.*			
	A15	2003/0003679	01/02/2003	Doyle *et al.*			
	A16	2003/0013323	01/16/2003	Hammond *et al.*			
	A17	2003/0025131	02/06/2003	Lee *et al.*			
	A18	2003/0034529	02/20/2003	Fitzgerald *et al.*			
	A19	2003/0041798	03/06/2003	Wenski *et al.*			
	A20	2003/0057439	03/27/2003	Fitzgerald			
	A21	2003/0077867	04/24/2003	Fitzgerald			
	A22	2003/0102498	06/05/2003	Braithwaite *et al.*			
	A23	2003/0127646	07/10/2003	Christiansen *et al.*			
	A24	2003/0186073	10/02/2003	Fitzgerald			03/18/2003
	A25	4,010,045	03/01/1977	Ruehrwein			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A26	4,710,788	12/01/1987	Dambkes *et al.*			
	A27	4,900,372	12/13/1990	Lee *et al.*			
	A28	4,987,462	01/22/1991	Kim *et al.*			
	A29	4,990,979	02/05/1991	Otto			
	A30	4,997,776	03/05/1991	Harame *et al.*			
	A31	5,013,681	05/07/1991	Godbey *et al.*			
	A32	5,091,767	02/25/1992	Bean *et al.*			
	A33	5,097,630	03/24/1992	Maeda *et al.*			
	A34	5,155,571	10/13/1992	Wang *et al.*			
	A35	5,159,413	10/27/1992	Calviello *et al.*			
	A36	5,166,084	11/24/1992	Pfiester			
	A37	5,177,583	01/05/1993	Endo *et al.*			
	A38	5,202,284	04/13/1993	Kamins *et al.*			
	A39	5,207,864	05/04/1993	Bhat *et al.*			
	A40	5,208,182	05/04/1993	Narayan *et al.*			
	A41	5,210,052	05/11/1993	Takasaki			
	A42	5,212,110	05/18/1993	Pfiester *et al.*			
	A43	5,221,413	06/22/1993	Brasen *et al.*			
	A44	5,241,197	08/31/1993	Murakami *et al.*			
	A45	5,250,445	10/05/1993	Bean *et al.*			
	A46	5,252,173	10/12/1993	Inoue			
	A47	5,279,687	01/18/1994	Tuppen *et al.*			
	A48	5,285,086	02/08/1994	Fitzgerald			-
	A49	5,291,439	03/01/1994	Kauffmann *et al.*			
	A50	5,298,452	03/29/1994	Meyerson			
	A51	5,308,444	05/03/1994	Fitzgerald *et al.*			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A52	5,310,451	05/10/1994	Tejwani *et al.*			
	A53	5,316,958	05/31/1994	Meyerson			
	A54	5,346,848	09/13/1994	Grupen-Shemansky *et al.*			
	A55	5,374,564	12/20/1994	Bruel			
	A56	5,399,522	03/21/1995	Ohori			
	A57	5,413,679	05/09/1995	Godbey			
	A58	5,424,243	06/13/1995	Takasaki			
	A59	5,425,846	06/20/1995	Koze *et al.*			
	A60	5,426,069	06/20/1995	Selvakumar *et al.*			
	A61	5,426,316	06/20/1995	Mohammad			
	A62	5,442,205	08/15/1995	Brasen *et al.*			
	A63	5,461,243	10/24/1995	Ek *et al.*			
	A64	5,461,250	10/24/1995	Burghartz *et al.*			
	A65	5,462,883	10/31/1995	Dennard *et al.*			
	A66	5,476,813	12/19/1995	Naruse			
	A67	5,479,033	12/26/1995	Baca *et al.*			
	A68	5,484,664	01/16/1996	Kitahara *et al.*			
	A69	5,523,243	06/04/1996	Mohammad			
	A70	5,523,592	06/04/1996	Nakagawa *et al.*			
	A71	5,534,713	07/09/1996	Ismail *et al.*			
	A72	5,536,361	07/16/1996	Kondo *et al.*			
	A73	5,540,785	07/30/1996	Dennard *et al.*			
	A74	5,596,527	01/21/1997	Tomioka *et al.*			
	A75	5,617,351	04/01/1997	Bertin *et al.*			
	A76	5,630,905	05/20/1997	Lynch *et al.*			
	A77	5,633,516	05/27/1997	Mishima *et al.*			
	A78	5,659,187	08/19/1997	Legoues *et al.*			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A79	5,683,934	11/04/1997	Candelaria			
	A80	5,698,869	12/16/1997	Yoshimi *et al.*			
	A81	5,714,777	02/03/1998	Ismail *et al.*			
	A82	5,728,623	03/17/1998	Mori			
	A83	5,739,567	04/14/1998	Wong			
	A84	5,759,898	06/02/1998	Ek *et al.*			
	A85	5,777,347	07/07/1998	Bartelink			
	A86	5,786,612	07/28/1998	Otani *et al.*			
	A87	5,786,614	07/28/1998	Chuang *et al.*			
	A88	5,792,679	08/11/1998	Nakato			
	A89	5,801,085	09/01/1998	Kim *et al.*			
	A90	5,808,344	09/15/1998	Ismail *et al.*			
	A91	5,810,924	09/22/1998	Legoues *et al.*			
	A92	5,828,114	10/27/1998	Kim *et al.*			
	A93	5,847,419	12/08/1998	Imai *et al.*			
	A94	5,859,864	01/12/1999	Jewell			
	A95	5,877,070	03/02/1999	Goesele *et al.*			
	A96	5,891,769	04/06/1999	Liaw *et al.*			
	A97	5,906,708	05/25/1999	Robinson *et al.*			
	A98	5,906,951	05/25/1999	Chu *et al.*			
	A99	5,912,479	06/15/1999	Mori *et al.*			
	A100	5,943,560	08/24/1999	Chang *et al.*			
	A101	5,963,817	10/05/1999	Chu *et al.*			
	A102	5,966,622	10/12/1999	Levine *et al.*			
	A103	5,998,807	12/07/1999	Lustig *et al.*			
	A104	6,010,937	01/04/2000	Karam *et al.*			
	A105	6,013,134	01/11/2000	Chu *et al.*			
	A106	6,030,884	02/29/2000	Mori			
	A107	6,033,974	03/07/2000	Henley *et al.*			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A108	6,033,995	03/07/2000	Muller			
	A109	6,039,803	03/21/2000	Fitzgerald *et al.*			
	A110	6,058,044	05/02/2000	Sugiura *et al.*			
	A111	6,059,895	05/09/2000	Chu *et al.*			
	A112	6,074,919	06/13/2000	Gardner *et al.*			
	A113	6,096,590	08/01/2000	Chan *et al.*			
	A114	6,103,559	08/15/2000	Gardner *et al.*			
	A115	6,107,653	08/22/2000	Fitzgerald			
	A116	6,111,267	08/29/2000	Fischer *et al.*			
	A117	6,117,750	09/12/2000	Bensahel *et al.*			
	A118	6,124,614	09/26/2000	Ryum *et al.*			
	A119	6,130,453	10/10/2000	Mei *et al.*			
	A120	6,133,799	10/17/2000	Favors *et al.*			
	A121	6,140,687	10/31/2000	Shimomura *et al.*			
	A122	6,143,636	11/07/2000	Forbes *et al.*			
	A123	6,153,495	11/28/2000	Kub *et al.*			
	A124	6,154,475	11/28/2000	Soref *et al.*			
	A125	6,160,303	12/12/2000	Fattaruso			
	A126	6,162,688	12/19/2000	Gardner *et al.*			
	A127	6,184,111	02/06/2001	Henley *et al.*			
	A128	6,191,006	02/20/2001	Mori			
	A129	6,191,007	02/20/2001	Matsui *et al.*			
	A130	6,191,432	02/20/2001	Sugiyama *et al.*			
	A131	6,194,722	02/27/2001	Fiorini *et al.*			
	A132	6,204,529	03/20/2001	Lung *et al.*			
	A133	6,207,977	03/27/2001	Augusto			
	A134	6,210,988	04/03/2001	Howe *et al.*			
	A135	6,218,677	04/17/2001	Broekaert			
	A136	6,232,138	05/15/2001	Fitzgerald *et al.*			
	A137	6,235,567	05/22/2001	Huang			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A138	6,242,324	06/05/2001	Kub *et al.*			
	A139	6,249,022	06/19/2001	Lin *et al.*			
	A140	6,251,755	06/26/2001	Furukawa *et al.*			
	A141	6,261,929	07/17/2001	Gehrke *et al.*			
	A142	6,266,278	07/24/2001	Harari *et al.*			
	A143	6,271,551	08/07/2001	Schmitz *et al.*			
	A144	6,271,726	08/07/2001	Fransis *et al.*			
	A145	6,291,321	09/18/2001	Fitzgerald			
	A146	6,313,016	11/06/2001	Kibbel *et al.*			
	A147	6,316,301	11/13/2001	Kant			
	A148	6,323,108	11/27/2001	Kub *et al.*			
	A149	6,329,063	12/11/2001	Lo *et al.*			
	A150	6,335,546	01/01/2002	Tsuda *et al.*			
	A151	6,339,232	01/15/2002	Takagi			
	A152	6,350,993	02/26/2002	Chu *et al.*			
	A153	6,368,733	04/09/2002	Nishinaga			
	A154	6,372,356	04/16/2002	Thornton *et al.*			
	A155	6,399,970	06/04/2002	Kubo *et al.*			
	A156	6,403,975	06/11/2002	Brunner *et al.*			
	A157	6,406,589	06/18/2002	Yanagisawa			
	A158	6,407,406	06/18/2002	Tezuka			
	A159	6,420,937	07/16/2002	Akatsuka *et al.*			
	A160	6,425,951	07/30/2002	Chu *et al.*			
	A161	6,429,061	08/06/2002	Rim			
	A162	6,482,749	11/19/2002	Billington *et al.*			
	A163	6,503,773	01/07/2003	Fitzgerald			
	A164	6,515,335	02/04/2003	Christiansen *et al.*			
	A165	6,518,644	02/11/2003	Fitzgerald			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A166	6,521,041	02/18/2003	Wu *et al.*			
	A167	6,525,338	02/25/2003	Mizushima *et al.*			
	A168	6,555,839	04/29/2003	Fitzgerald			
	A169	6,573,126	06/03/2003	Cheng *et al.*			
	A170	6,576,532	06/10/2003	Jones *et al.*			
	A171	6,583,015	06/24/2003	Fitzgerald *et al.*			
	A172	6,593,191	07/15/2003	Fitzgerald			
	A173	6,594,293	07/15/2003	Bulsara *et al.*			
	A174	6,602,613	08/05/2003	Fitzgerald			
	A175	6,603,156	08/05/2003	Rim			

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B1	41 01 167	07/23/1992	DE				N	Abstract
	B2	0 514 018	11/19/1992	EP				N	Y
	B3	0 587 520	03/16/1994	EP				N	Y
	B4	0 683 522	11/22/1995	EP				N	Y
	B5	0 828 296	03/11/1998	EP				N	Y
	B6	0 829 908	03/18/1998	EP				N	Y
	B7	0 838 858	04/29/1998	EP				N	Abstract
	B8	1 020 900	07/19/2000	EP				N	Y
	B9	1 174 928	01/23/2002	EP				N	Y
	B10	2 342 777	04/19/2000	GB				Y	Y
	B11	4-307974	10/30/1992	JP				N	Abstract

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B12	5-166724	07/02/1993	JP				N	Abstract
	B13	6-177046	06/24/1994	JP				N	Abstract
	B14	6-244112	09/02/1994	JP				Y	Y
	B15	6-252046	09/09/1994	JP				Y	Y
	B16	7-94420	04/07/1995	JP				N	Abstract
	B17	7-106446	04/21/1995	JP				N	Abstract
	B18	7-240372	09/12/1995	JP				N	Abstract
	B19	10-270685	10/09/1998	JP				N	Y
	B20	11-233744	08/27/1999	JP				N	Abstract
	B21	63-73398	04/02/1988	JP				N	N
	B22	2000-021783	01/21/2000	JP				N	Y
	B23	2000-031491	01/28/2000	JP				N	Y
	B24	2000-513507	10/10/2000	JP				Y	Y
	B25	2001-319935	11/16/2001	JP				N	Y
	B26	2002-076334	03/15/2002	JP				N	Y
	B27	2002-164520	06/07/2002	JP				N	Y
	B28	2002-289533	10/04/2002	JP				N	Y
	B29	2002-356399	12/13/2002	JP				N	Y
	B30	2003-520444	07/02/2003	JP				N	Abstract
	B31	98/59365	12/30/1998	WO				N	Y
	B32	99/53539	10/21/1999	WO				N	Y
	B33	00/48239	08/17/2000	WO				N	Y
	B34	00/54338	09/14/2000	WO				N	Y
	B35	01/022482	03/29/2001	WO				N	Y
	B36	01/54175	07/26/2001	WO				N	Y

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B37	01/54202	07/26/2001	WO				N	Y
	B38	01/93338	12/06/2001	WO				N	Y
	B39	01/99169	12/27/2001	WO				N	Y
	B40	02/071488	09/12/2002	WO				N	Y
	B41	02/071491	09/12/2002	WO				N	Y
	B42	02/071495	09/12/2002	WO				N	Y
	B43	02/082514	10/17/2002	WO				N	Y
	B44	02/13262	02/14/2002	WO				N	Y
	B45	02/15244	02/21/2002	WO				N	Y
	B46	02/27783	04/04/2002	WO				N	Y
	B47	02/47168	06/13/2002	WO				N	Y
	B48	03/015140	02/20/2003	WO				N	Y

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C1	Armstrong *et al.*, "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEDM Technical Digest (1995 International Electron Devices Meeting), pp. 761-764.
	C2	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices," PhD Thesis, Massachusetts Institute of Technology, 1999, pp. 1-154.
	C3	Augusto *et al.*, "Proposal for a New Process Flow for the Fabrication of Silicon-Based Complementary MOD-MOSFETs without Ion Implantation," Thin Solid Films, Vol. 294, No. 1-2 (February 15, 1997), pp. 254-258.
	C4	Barradas *et al.*, "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," Modern Physics Letters B, Vol. 15 (2001), abstract.
	C5	Borenstein *et al.*, "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," Proceedings of the 1999 12th IEEE International Conference on Micro Electro Mechanical Systems (MEMs) (January 17-21, 1999), pp. 205-210.
	C6	Bouillon *et al.*, "Search for the optimal channel architecture for 0.18/0.12 μm bulk CMOS experimental study," IEEE (1996), pp. 21.2.1-21.2.4.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C7	Bruel *et al.*, "®SMART CUT: A Promising New SOI Material Technology," Proceedings of the 1995 IEEE International SOI Conference (October 1995), pp. 178-179.
	C8	Bruel, "Silicon on Insulator Material Technology," Electronic Letters, Vol. 13, No. 14 (July 6, 1995), pp. 1201-1202.
	C9	Bufler *et al.*, "Hole transport in strained Si1-xGex alloys on Si1-yGey substrates," Journal of Applied Physics, Vol. 84, No. 10 (November 15, 1998), pp. 5597-5602.
	C10	Bulsara *et al.*, "Relaxed $In_xGa_{1-x}As$ Graded Buffers Grown with Organometallic Vapor Phase Epitaxy on GaAs," Applied Physics Letters, Vol. 72, Issue 13 (July 30, 1998), pp. 1608-1610.
	C11	Bulsara, "Materials Issues with the Integration of Lattice-Mismatched $In_xGa_{1-x}As$ on GaAs," PhD Thesis, MIT, June 1998, pp. 1-178.
	C12	Burghartz *et al.*, "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 1 (January 1996), pp. 100-104.
	C13	Buttard *et al.*, "Toward Two-Dimensional Self-Organization of Nanostructures Using Wafer Bonding and Nanopatterned Silicon Surfaces," IEEE – 2002 Journal of Quantum Electronics, Vol. 38, Issue 8 (August 2002), pp. 995-1005.
	C14	Canaperi *et al.*, "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with strained epitaxial films," International Business Machines Corporation, USA (2002), abstract.
	C15	Carlin *et al.*, "High Efficiency GaAs-on-Si Solar Cells with High Voc using Graded Gesi Buffers," IEEE – 2000 (2000), pp. 1006-1011.
	C16	Carlin *et al.*, "Investigation and Development of High Quality GaAs-on-Si for Space Photovoltaics Using a Graded GeSi," PhD Thesis, Ohio State University, 2001, pp. 1-232.
	C17	Chang *et al.*, "Selective Etching of SiGe/Si Heterostructures," Journal of the Electrochemical Society, No. 1 (January 1991), pp. 202-204.
	C18	Charasse *et al.*, "MBE Growth of GaAs on Si at Thomson," Institute of Electronic Structure and Laser
	C19	Cheng *et al.*, "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," IEEE Electron Device Letters, Vol. 22, No. 7 (July 2001), pp. 321-323.
	C20	Cheng *et al.*, "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," Journal of Electronic Materials, Vol. 30, No. 12 (2001), pp. L37-L39.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C21	Crumbaker *et al.*, "The Influence of Dislocation Density on Electron Mobility in InP Films on Si," Applied Physics Letters, Vol. 59, Issue 9 (08/26/91), pp. 1090-1092.
	C22	Cullis *et al.*, "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," Journal of Vacuum Science and Technology A, Vol. 12, No. 4 (July/August 1994), pp. 1924-1931.
	C23	Currie *et al.*, "Carrier mobilities and process stability of strained Si n- and p-MOSFETs on SiGe virtual substrates," Journal of Vacuum Science and Technology B, Vol. 19, No. 6 (Nov/Dec 2001), pp. 2268-2279.
	C24	Currie *et al.*, "Controlling Threading Dislocation Densities in Ge on Si Using Graded SiGe Layers and Chemical-Mechanical Polishing," Applied Physics Letters, Vol. 72, Issue 14 (04/06/98), pp. 1718-1720.
	C25	Currie, "SiGe Virtual Substrate Engineering for Integration of III-V Materials, Microelectromechanical Systems and Strained Silicon Mosfets with Silicon," PhD Thesis, MIT, 2001, pp. 1-190.
	C26	Dilliway *et al.*, "Characterization of Morphology and Defects in Silicon Germanium Virtual Substrates," Journal of Materials Science, Vol. 11, Issue 7 (2000), pp. 549-556.
	C27	Eaglesham *et al.*, "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," Physical Review Letters, Vol. 64, No. 16 (April 16, 1990), pp. 1943-1946.
	C28	Erdtmann *et al.*, "Gainas/Inp Quantum Well Infrared Photodetectors on Si Substrate for Low-Cost Focal Plan Arrays," PhD Thesis, Northwestern University, 2000, pp. 1-225.
	C29	Feijoo *et al.*, "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," Journal of Electronic Materials, Vol. 23, No. 6 (June 1994), pp. 493-496.
	C30	Fischetti *et al.*, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," Journal of Applied Physics, Vol. 80, No. 4 (August 15, 1996), pp. 2234-2252.
	C31	Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electronmobility in thin-oxide structures," Journal of Applied Physics, Vol. 89, No. 2 (January 15, 2001), pp. 1232-1250.
	C32	Fitzgerald, "Dislocations in strained-layer epitaxy: theory, experiment, and applications," Materials Science Reports, Vol. 7 (1991), pp. 87-142.
	C33	Fitzgerald *et al.*, "Dislocation dynamics in relaxed graded composition semiconductors," Materials Science and Engineering, B67 (1999), pp. 53-61.
	C34	Fitzgerald *et al.*, "GeSi/Si Nanostructures," Department of Material Science, MIT (1995) pp 1-15
	C35	Fitzgerald *et al.*, "Relaxed GexSi1-x structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," Journal of Vacuum Science Technology, B 10(4) (Jul/August 1992), pp. 1807-1819.
	C36	Fitzgerald *et al.*, "Totally Relaxed GexSi1-x Layers with Low Threading Dislocation Densities Grown on Si Substrates," Applied Physics Letters, Vol. 59, No. 7 (August 12, 1991), pp. 811-813. -

EXAMINER	DATE CONSIDERED

FORM PTO - 1449	ATTORNEY DOCKET NO.: ASC-058B
INFORMATION DISCLOSURE STATEMENT	APPLICANT(S): Leitz *et al.*
	SERIAL NO.: 10/646,353
	FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C37	Garone *et al.*, "Silicon vapor phase epitaxial growth catalysis by the presence of germane," Applied Physics Letters, Vol. 56, No. 13 (March 26, 1990), pp. 1275-1277.
	C38	Giovane *et al.*, "Strain-Balanced Silicon-Germanium Materials for Near IR Photodetection in Silicon-Based Optical Interconnects," PhD Thesis, MIT, 1998, pp. 1-134.
	C39	Gray *et al.*, "Analysis and Design of Analog Integrated Circuits," John Wiley & Sons, 1984, pp. 605-632.
	C40	Groenert *et al.*, "Strategies for Direct Monolithic Integration of AlxGa(1-x)As/InxGa(1-x)As LEDS and Lasers on Ge/GeSi/Si Substrates Via Relaxed Graded GexSi(1-x) Buffer Layers," Materials Research Society Symposium Proceedings, Vol. 692 (2002), pp. H.9.30.1-H.9.30.6.
	C41	Grützmacher *et al.*, "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," Applied Physics Letters, Vol. 63, No. 18 (November 1, 1993), pp. 2531-2533.
	C42	Hackbarth *et al.*, "Alternatives to thick MBE-grown relaxed SiGe buffers," Thin Solid Films, Vol. 369, No. 1-2 (July 2000), pp. 148-151.
	C43	Hackbarth *et al.*, "Strain relieved SiGe buffers for Si-based heterostructure field-effect transistors," Journal of Crystal Growth, Vol. 201/202 (1999), pp. 734-738.
	C44	Herzog *et al.*, "SiGe-based FETs: buffer issues and device results," Thin Solid Films, Vol. 380 (2000), pp. 36-41.
	C45	Höck *et al.*, "Carrier mobilities in modulation doped Si1-xGex heterostructures with respect to FET applications," Thin Solid Films, Vol. 336 (1998), pp. 141-144.
	C46	Höck *et al.*, "High hole mobility in Si0.17 Ge0.83 channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," Applied Physics Letters, Vol. 76, No. 26 (June 26, 2000), pp. 3920-3922.
	C47	Höck *et al.*, "High performance 0.25 μm p-type Ge/SiGe MODFETs," Electronics Letters, Vol. 34, No. 19 (September 17, 1998), pp. 1888-1889.
	C48	Houghton, "Strain Relaxation Kinetics in $Si_{1-x}Ge_x/Si$ Heterostructures," Journal of Applied Physics, Vol. 70, No. 4 (August 15, 1991), pp. 2136-2151.
	C49	Hsu *et al.*, "Near Field Scanning Optical Microscopy Studies of Electronic and Photonic Materials and Devices," Materials Science and Engineering Reports: A Review Journal, Vol. 33 (2001), pp. 1-50.
	C50	Huang *et al.*, "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," Applied Physics Letters, Vol. 76, No. 19 (May 8, 2000), pp. 2680-2682.
	C51	Huang *et al.*, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits," IEEE Journal of Solid-State Circuits, Vol. 33, No. 7 (July 1998), pp. 1023-1036.
	C52	Ishikawa *et al.*, "Creation of Si-Ge-based SIMOX structures by low energy oxygen implantation," Proceedings of the 1997 IEEE International SOI Conference (October 1997), pp. 16-17.
	C53	Ishikawa *et al.*, "SiGe-on-insulator substrate using SiGe alloy grown Si(001)," Applied Physics Letters, Vol. 75, No. 7 (August 16, 1999), pp. 983-985.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C54	Ismail *et al.*, "Modulation-doped n-type Si/SiGe with inverted interface," Applied Physics Letters, Vol. 65, No. 10 (September 5, 1994), pp. 1248-1250.
	C55	Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington, D.C. (December 10, 1995), pp. 20.1.1-20.1.4.
	C56	Kearney *et al.*, "The effect of alloy scattering on the mobility of holes in a Si1-xGex quantum well," Semiconductor Science and Technology, Vol. 13 (1998), pp. 174-180.
	C57	Kim *et al.*, "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier," IEEE Microwave and Guided Wave Letters, Vol. 8, No. 8 (August 1998), pp. 293-295.
	C58	Kissinger *et al.*, "Stepwise Equilibrated Graded GexSi1x Buffer with Very Low Threading Dislocation Density on SI(001)," American Institute of Physics / Applied Physics Letters, Vol. 66, Issue 16 (April 17, 1995), pp. 2083-2085.
	C59	Knall *et al.*, "The Use of Graded in GaAs Layers and Patterned Substrates to Remove Threading Dislocations From GaAs on Si," Journal of Applied Physics, Vol. 76, Issue 5 (September 1, 1994), pp. 2697-2702.
	C60	Koester *et al.*, "Extremely High Transconductance Ge/Si0.4Ge0.6 p-MODFET's Grown by UHV-CVD," IEEE Electron Device Letters, Vol. 21, No. 3 (March 2000), pp. 110-112.
	C61	König *et al.*, "Design Rules for n-Type SiGe Hetero FETs," Solid State Electronics, Vol. 41, No. 10 (1997), pp. 1541-1547.
	C62	König *et al.*, "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters, Vol. 14, No. 4 (April 1993), pp. 205-207.
	C63	König *et al.*, "SiGe HBTs and HFETs," Solid-State Electronics, Vol. 38, No. 9 (1995), pp. 1595-1602.
	C64	Kummer *et al.*, "Low energy plasma enhanced chemical vapor deposition," Materials Science and Engineering, B89 (2002), pp. 288-295.
	C65	Kuznetsov *et al.*, "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," Journal of Vacuum Science and Technology, B 13(6) (November/December 1995), pp. 2892-2896.
	C66	Langdo, "High Quality Ge on Si by Epitaxial Necking," Applied Physics Letters, Vol. 76, Issue 25 (June 19, 2000), pp. 3700-3702.
	C67	Larson, "Integrated Circuit Technology Options for RFIC's Present Status and Future Directions," IEEE Journal of Solid-State Circuits, Vol. 33, No. 3 (March 1998), pp. 387-399.
	C68	Lee *et al.*, "CMOS RF Integrated Circuits at 5 GHz and Beyond," Proceedings of the IEEE, Vol. 88, No. 10 (October 2000), pp. 1560-1571.
	C69	Lee *et al.*, "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Si1-xGex/Si virtual substrates," Applied Physics Letters, Vol. 79, No. 20 (November 12, 2001), pp. 3344-3346.
	C70	Lee *et al.*, "Strained Ge channel p-type MOSFETs fabricated on Si1-xGex/Si virtual substrates," Materials Research Society Symposium Proceedings, Vol. 686 (2002), pp. A1.9.1-A1.9.5.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C71	LeGoues *et al.*, "Relaxation of SiGe Thin Films Grown on Si/SiO2 Substrates," Journal of Applied Physics, Vol. 75, Issue 11 (June 1, 1974), pp. 2730-2738.
	C72	Leitz *et al.*, "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Materials Research Society Symposium Proceedings, Vol. 686 (2002), pp. A3.10.1-A3.10.6.
	C73	Leitz *et al.*, "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," Journal of Applied Physics, Vol. 90, No. 6 (September 15, 2001), pp. 2730-2736.
	C74	Leitz *et al.*, "Hole mobility enhancements in strained Si/Si1-yGey p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si1-xGex (x<y) virtual substrates," Applied Physics Letters, Vol. 79, No. 25 (December 17, 2001), pp. 4246-4248.
	C75	Li *et al.*, "Design of high speed Si/SiGe heterojunction complementary metal-oxide-semiconductor field effect transistors with reduced short-channel effects," Journal of Vacuum Science and Technology A, Vol. 20, No.3 (May/June 2002), pp. 1030-1033.
	C76	Liu *et al.*, "Growth Study of Surfactant-Mediated Relaxed SiGe Graded Layers for 1.55-μM Photodetector Applications," Thin Solid Films, Vol. 380, Issue 1-2 (2000), pp. 54-56.
	C77	Liu *et al.*, "High-Quality Ge Films on Si Substrates Using SB Surfactant-Mediated Graded SiGe Buffers," Applied Physics Letters, Vol. 79, Issue 21 (November 19, 2001), pp. 3431-3433.
	C78	Luan *et al.*, "High Quality Ge Epilayers on Si with Low Threading-Dislocations Densities," Applied Physics Letters, Vol. 75, Issue 19 (November 8, 1999), pp. 2909-2911.
	C79	Lu *et al.*, "High Performance 0.1 μm Gate-Length P-Type SiGe MODFET's and MOS-MODFET's," IEEE Transactions on Electron Devices, Vol. 47, No. 8 (August 2000), pp. 1645-1652.
	C80	Luo *et al.*, "High-Quality Strain-Relaxed SiGe Films Grown with Low Temperature Si Buffer," Journal of Applied Physics, Vol. 89, Issue 13 (September 23, 1991), pp. 1611-1613.
	C81	Maiti *et al.*, "Strained-Si heterostructure field effect transistors," Semiconductor Science and Technology, Vol. 13 (1998), pp. 1225-1246.
	C82	Maszara, "Silicon-On-Insulator by Wafer Bonding: A Review," Journal of the Electrochemical Society, No. 1 (January 1991), pp. 341-347.
	C83	Meyerson *et al.*, "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," Applied Physics Letters, Vol. 53, No. 25 (December 19, 1988), pp. 2555-2557.
	C84	Mizuno *et al.*, "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS-Electron/Hole Mobility Enhancement," 2002 Symposium on VLSI Technology, Honolulu (June 13-15), IEEE New York, pp. 210-211.
	C85	Mizuno *et al.*, "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE Electron Device Letters, Vol. 21, No. 5 (May 2000), pp. 230-232.
	C86	Mizuno *et al.*, "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE IDEM Technical Digest (1999 International Electron Device Meeting), pp. 934-936.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C87	Momose *et al.*, "Dislocation-Free and Lattice-Matched Si/GAP1-xNx/Si Structure for Photo-Electronic Integrated Systems," Applied Physics Letters, Vol. 79, Issue 25 (December 17, 2001), pp. 4151-4153.
	C88	Monroe *et al.*, "Comparison of Mobility-Limiting Mechanisms in High-Mobility Si1-xGex Heterostructures," Journal of Vacuum Science and Technology B, Vol. B11, Issue 4 (Jul/Aug 1993), pp. 1731-1737.
	C89	Nayak *et al.*, "High-Mobility Strained-Si PMOSFET's," IEEE Transactions on Electron Devices, Vol. 43, No. 10 (October 1996), pp. 1709-1716.
	C90	Oh *et al.*, "Interdigitated Ge P-I-N Photodetectors Fabricated on a Si Substrate Using Graded SiGe Buffer Layers," IEEE – Journal of Quantum Electronics, Vol. 38, Issue 9 (Sept 2002), pp. 1238-1241.
	C91	Ohori *et al.*, "Effect of Threading Dislocations on Mobility in Selectively Doped Heterostructures Grown on Si Substrates," Journal of Applied Physics, Vol. 75, Issue 7 (April 1, 1994), pp. 3681-3683.
	C92	O'Neill *et al.*, "SiGe virtual substrate N-channel heterojunction MOSFETS," Semiconductor Science and Technology, Vol. 14 (1999), pp. 784-789.
	C93	Ota, "Application of heterojunction FET to power amplifier for cellular telephone," Electronic Letters, Vol. 30, No. 11(May 26, 1994), pp. 906-907.
	C94	Papananos, "Radio-Frequency Microelectronic Circuits for Telecommunication Applications," Kluwer Academic Publishers, 1999, pp. 115-117, 188-193.
	C95	Parker *et al.*, "SiGe heterostructure CMOS circuits and applications," Solid State Electronics, Vol. 43 (1999), pp. 1497-1506.
	C96	Powell *et al.*, "New Approach to the Growth of Low Dislocation Relaxed SiGe Material," Applied Physics Letters, Vol. 64, Issue 14 (April 4, 1994), pp.1856-1858.
	C97	Ransom *et al.*, "Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's," IEEE Transactions on Electron Devices, Vol. 38, No. 12 (December 1991), pp. 2695.
	C98	Reinking *et al.*, "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," Electronics Letters, Vol. 35, No. 6 (March 18, 1999), pp. 503-504.
	C99	Rim, "Application of Silicon-Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field-Effect Transistors," PhD Thesis, Stanford University, 1999, pp. 1-184.
	C100	Rim *et al.*, "Enhanced Hole Mobilities in Surface-Channel Strained-Si p-MOSFETs," IEDM (1995), pp. 517-520.
	C101	Rim *et al.*, "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," IEEE Transactions on Electron Devices, Vol. 47, No. 7 (July 2000), pp. 1406-1415.
	C102	Robbins *et al.*, "A model for heterogeneous growth of Si1-xGex films for hydrides," Journal of Applied Physics, Vol. 69, No. 6 (March 15, 1991), pp. 3729-3732.
	C103	Sadek *et al.*, "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEEE Transactions on Electron Devices (August 1996), pp. 1224-1232.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C104	Sakaguchi *et al.*, "ELTRAN® by Splitting Porous Si Layers," Proceedings of the 195th International SOI Symposium, Vol. 99-3 (1999), pp. 117-121.
	C105	Sakai *et al.*, "Reduction of Threading Dislocation Density in SiGe Layers on Si (001) Using a Two-Step Strain – Relaxation Procedure," Applied Physics Letters, Vol. 79, Issue 21 (November 19, 2001), pp. 3398-3400.
	C106	Samavedam *et al.*, "Novel Dislocation Structure and Surface Morphology Effects in Relaxed Ge/Si-Ge (graded) / Si Structures," Journal of Applied Physics, Vol. 87, Issue 7 (April 1, 1997), pp. 3108-3116.
	C107	Schäffler, "High-Mobility Si and Ge Structures," Semiconductor Science and Technology, Vol. 12 (1997), pp. 1515-1549.
	C108	Schimmel, "Defect Etch for <100> Silicon Evaluation," Journal of the Electrochemical Society, Vol. 126, No. 3 (March 1979), pp. 479-482.
	C109	Sugimoto *et al.*, "A 2V, 500 MHz and 3V, 920 MHz Low-Power Current-Mode 0.6 μm CMOS VCO Circuit," IEICE Trans Electron, Vol.E82-C, No. 7 (July 1999), pp. 1327-1329.
	C110	Taylor *et al.*, "Optoelectronic Device Performance on Reduced Threading Dislocation Density GaAs/Si," American Institute of Physics, Vol. 89, Issue 8 (April 15, 2001), pp.4365-4375.
	C111	Tement *et al.*, "Metal Gate Strained Silicon MOSFETs for Microwave Integrated Circuits," IEEE (October 2000), pp. 38-43.
	C112	Ting *et al.*, "Monolithic Integration of III-V Materials and Devices on Silicon," SPIE Conference 1999-Silicon Based Optoelectronics, Vol. 3630 (Jan 1999), pp.19-28.
	C113	Tsang *et al.*, "Measurements of alloy composition and strain in thin Ge_xSi_{1-x} layers," Journal of Applied Physics, Vol. 75, No. 12 (June 15, 1994), pp. 8098-8108.
	C114	Tweet *et al.*, "Factors determining the composition of strained GeSi layers grown with disilane and germane," Applied Physics Letters, Vol. 65, No. 20 (November 14, 1994), pp. 2579-2581.
	C115	Usami *et al.*, "Spectroscopic study of Si-based quantum wells with neighboring confinement structure," Semiconductor Science and Technology, (1997), abstract.
	C116	Valtuena *et al.*, "Influence of the Surface Morphology on the Relaxation of Low-Strained InxGa1-x As Linear Buffer Structures," Journal of Crystal Growth, Vol. 182 (1997), pp. 281-291.
	C117	Watson *et al.*, "Relaxed, Low Threading Defect Density Si0.7Ge0.3 Epitaxial Layers Grown on Si by Rapid Thermal Chemical Vapor Deposition," Journal of Applied Physics, Vol. 75, Issue 1 (January 1, 1994), pp. 263-269.
	C118	Welser *et al.*, "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," IEEE Electron Device Letters, Vol. 15, No. 3 (March 1994), pp. 100-102.
	C119	Welser *et al.*, "Evidence of Real-Space Hot-Electron Transfer in High Mobility, Strained-Si Multilayer MOSFETs," IEEE IDEM Technical Digest (1993 International Electron Devices Meeting), pp. 545-548.

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-058B APPLICANT(S): Leitz *et al.* SERIAL NO.: 10/646,353 FILING DATE: August 22, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C120	Welser *et al.*, "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEEE IDEM Technical Digest (1992 International Electron Devices Meeting), pp. 1000-1002.
	C121	Welser, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors," PhD Thesis, Stanford University, 1994, pp. 1-205.
	C122	Wolf *et al.*, "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA, 1986, pp. 384-386.
	C123	Xie *et al.*, "Fabrication of High Mobility Two-Dimensional Electron and Hole Gases in GeSi/Si," Journal of Applied Physics, Vol. 73, Issue 12 (June 15, 1993), pp. 8364-8370.
	C124	Xie *et al.*, "Semiconductor Surface Roughness: Dependence on Sign and Magnitude of Bulk Strain," The Physical Review Letters, Vol. 73, No. 22 (November 28, 1994), pp. 3006-3009.
	C125	Xie *et al.*, "Very High Mobility Two-Dimensional Hole Gas in Si/GexSi1-x/Ge Structures Grown by Molecular Beam Epitaxy," Applied Physics Letters, Vol. 63, Issue 16 (October 18, 1993), pp. 2263-2264.
	C126	Xie, "SiGe Field Effect Transistors," Materials Science and Engineering, Vol. 25 (1999), pp. 89-121.
	C127	Yamagata *et al.*, "Bonding, Splitting and Thinning by Porous Si in ELTRAN®; SOI-Epi Wafer™," Materials Research Society Symposium Proceedings, Vol. 681E (2001), pp. I8.2.1-I8.2.10.
	C128	Yeo *et al.*, "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel," IEEE Electron Device Letters, Vol. 21, No. 4 (April 2000), pp. 161-163.
	C129	Zhang *et al.*, "Demonstration of a GaAs-Based Compliant Substrate Using Wafer Bonding and Substrate Removal Techniques," Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, University Park, PA 16802, 1998, pp. 25-28.
	C130	"Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates," IBM Technical Disclosure Bulletin, Vol. 32, No. 8A (January 1990), pp. 330-331.
	C131	"2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," IBM Technical Disclosure Bulletin, Vol. 35, No. 4B (September 1992), pp. 136-140.

EXAMINER	DATE CONSIDERED

2729587